Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Canceled)

2-30. (Previously Canceled)

31. (New) A NAND flash memory comprising:

a NAND memory cell array having a NAND block which comprises NAND memory cells;

first and second lines arranged in the NAND block with a first interval, connected to the NAND memory cells; and

third and fourth lines arranged with a second interval wider than the first interval; wherein

the first interval is a minimum interval less than 0.12 μm, and a maximum value of a voltage generated between the third and fourth lines is greater than a maximum value of a voltage generated between the first and second lines.

32. (New) The NAND flash memory according to claim 31, wherein the second line is connected to a first contact plug having the width larger than that of the second line, and the distance between the first line and the first contact plug is narrower than the first interval.

33. (New) The NAND flash memory according to claim 32, wherein the fourth line is connected to a second contact plug having the width larger than that of the fourth line, and the distance between the third line and the second contact plug is narrower than the second interval.

34. (New) The NAND flash memory according to claim 31, wherein the first and second line and the third and fourth lines are formed on the same wiring layer.

35. (New) The NAND flash memory according to claim 31, wherein the first and second line and the third and fourth lines are formed on a different wiring layer.

36. (New) The NAND flash memory according to claim 31, wherein the first and second lines are word lines.

37. (New) The NAND flash memory according to claim 31, wherein the first and second lines are bit lines.

38. (New) The NAND flash memory according to claim 31, wherein when the first interval is assumed to be S1, the maximum value of the voltage generated between the first and second lines is assumed to be V1 and the maximum value of the voltage generated between the third and fourth lines is assumed to be V2, the second interval S2 is expressed by $S2 = (V2/V1) \times S1$.

39. (New) The NAND flash memory according to claim 33, wherein when the distance between the first line and the first contact plug is assumed to be Sa, the maximum value of the voltage generated between the first and second lines is assumed to be V1 and the maximum value of the voltage generated between the third and fourth lines is assumed to be V2, the distance Sb between the third line and the second contact plug is expressed by $Sb = (V2/V1) \times Sa$.

40. (New) The NAND flash memory according to claim 31, wherein when a power supply potential is assumed to be Vcc, a ground potential is assumed to be Vss, an erase potential is assumed to be Vera and a forward bias voltage between a well area and a diffusion layer is assumed to be Vf, the maximum value Vmax1 of the voltage generated between the first and second lines is expressed by Vmax1 = Vcc-Vss and the maximum value Vmax2 of the voltage generated between the third and fourth lines is expressed by Vmax2 = (Vera-Vf) -Vcc.

41. (New) A NAND flash memory comprising:

a NAND memory cell array having a NAND block which comprises NAND memory cells;

first and second lines arranged in the NAND block with a first interval, connected to the NAND memory cells;

a third line, wherein a second interval between the first and third lines is wider than the first interval; and

a first transistor configured to connect the second and third lines; wherein

the first interval is a minimum interval less than 0.12 μm, and a maximum value of a voltage generated between the first and third lines is greater than a maximum value of a voltage generated between the first and second lines.

42. (New) The NAND flash memory according to claim 41, wherein the second line is connected to the first transistor through the wiring layer formed just under the second line, and the third line is connected to the first transistor through the wiring layer formed just under the third line.

43. (New) The NAND flash memory according to claim 41, wherein the first and second lines are word lines.

44. (New) The NAND flash memory according to claim 41, wherein the first and second lines are bit lines.

45. (New) The NAND flash memory according to claim 41, wherein the third line is a line to give a predetermined potential to the second line, during read operation.

46. (New) The NAND flash memory according to claim 41, wherein the third line is a line to connect the second line to a sense amplifier.

47. (New) The NAND flash memory according to claim 41, wherein the transistor turns off, the first and second line has an erase potential and the third line has a power supply potential, during erase operation.

48. (New) The NAND flash memory according to claim 41, wherein when the first interval is assumed to be S1, the maximum value of the voltage generated between the first and second lines is assumed to be V1 and the maximum value of the voltage generated between the first and third lines is assumed to be V2, the second interval S2 is expressed by $S2 = (V2/V1) \times S1$.

49. (New) The NAND flash memory according to claim 41, wherein when a power supply potential is assumed to be Vcc, a ground potential is assumed to be Vss, an erase potential is assumed to be Vera and a forward bias voltage between a well area and a diffusion layer is assumed to be Vf, the maximum value Vmax1 of the voltage generated between the first and second lines is expressed by Vmax1 = Vcc-Vss and the maximum value Vmax2 of the voltage generated between the first and third lines is expressed by Vmax2 = (Vera-Vf) -Vcc.

50. (New) The NAND flash memory according to claim 41, wherein the second line is connected to a first contact plug having the width larger than that of the second line, and the distance between the first line and the first contact plug is narrower than the first interval.

51. (New) The NAND flash memory according to claim 50, wherein the third line is connected to a second contact plug having the width larger than that of the third line, and the distance between the first line and the second contact plug is narrower than the second interval.

52. (New) The NAND flash memory according to claim 51, wherein when the distance between the first line and the first contact plug is assumed to be Sa, the maximum value of the voltage generated between the first and second lines is assumed to be V1 and the maximum value of the voltage generated between the first and third lines is assumed to be V2, the distance Sb between the first line and the second contact plug is expressed by $Sb = (V2/V1) \times Sa$.

53. (New) The NAND flash memory according to claim 41, further comprising a second transistor connected to the first line; wherein

the first and second transistors are arranged in being adjacent in the extending direction of the first and second lines.

54. (New) The NAND flash memory according to claim 53, wherein the second transistor is connected to between the first and third lines.

55. (New) A NAND flash memory comprising:

a NAND memory cell array having a NAND block which comprises NAND memory cells;

first and second lines arranged in the NAND block with a first interval, connected to the NAND memory cells;

a third line; and

a first transistor configured to connect the second and third lines; wherein

the first interval is a minimum interval less than 0.12 μm, and a maximum value of a voltage generated between the first and third lines is greater than a maximum value of a voltage generated between the first and second lines, and the third line is arranged at a position not adjacent to the first line.

56. (New) The NAND flash memory according to claim 55, wherein the second line is connected to the first transistor through the wiring layer formed just under the second line, and the third line is connected to the first transistor through the wiring layer formed just under the third line.

57. (New) The NAND flash memory according to claim 55, wherein the first and second lines are word lines.

58. (New) The NAND flash memory according to claim 55, wherein the first and second lines are bit lines.

59. (New) The NAND flash memory according to claim 55, wherein the third line is a line to give a predetermined potential to the second line, during read operation.

60. (New) The NAND flash memory according to claim 55, wherein the third line is a line to connect the second line to a sense amplifier.

61. (New) The NAND flash memory according to claim 55, wherein the transistor turns off, the first and second line has an erase potential and the third line has a power supply potential, during erase operation.

62. (New) The NAND flash memory according to claim 55, further comprising a fourth line arranged in being adjacent to at least one of the first, second and third lines; wherein

the fourth line is a dummy line set to be floated its potential.